What is claimed is:

1. A microprocessor system comprising:

a bus for transferring information;

a memory, coupled to said bus, comprised of a type of memory device which is interchangeably a Burst Extended Data Out type memory device or a Fast Page Mode type memory device, said memory having a first set of access control signal timing requirements for the Burst Extended Data Out type memory device and a second set of access control signal timing requirements for the Fast Page Mode type memory device;

a programmable memory controller, coupled to said bus and to said memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to said memory; and

a microprocessor, coupled to said bus, said memory and said memory controller, responsive to information from said memory to program said memory controller to provide a set of access control signals to said memory in accordance with the type of memory device said memory is comprised of.

2. A microprocessor system comprising:

a bus for transferring information;

a memory, coupled to said bus, comprised of a type of memory device which is interchangeably a Burst Extended Data Out type memory device or a Extended Data Out type memory device, said memory having a first set of access control signal timing requirements for the Burst Extended Data Out type memory device and a second set of access control signal timing requirements for the Extended Data Out type memory device;

a programmable memory controller, coupled to said bus and to said memory, capable of providing the first set of access control signal timing

requirements and the second set of access control signal timing requirements to said memory;

a nonvolatile memory device coupled to said bus; and

a microprocessor, coupled to said bus and said memory controller, responsive to information from said memory and said nonvolatile memory device to program said memory controller to provide a set of access control signals to said memory in accordance with the type of memory device said memory is comprised of.

3. The system of claim 2, further comprising:

a power supply; and

a power up detection circuit coupled to said microprocessor and to said power supply, said power up detection circuit responsive to a signal from said power supply to cause said microprocessor to access said

nonvolatile memory device to receive information enabling said microprocessor to detect the type of memory device and to program the memory controller in accordance with the type of memory device said memory is comprised of.

4. A microprocessor system comprising:

a bus for transferring information;

a memory, coupled to said bus, comprised of a type of memory device which is selected from memory devices operable in first and second modes, said memory having a first set of access control signals for operation in said first mode and a second set of access control signals for operation in said second mode;

a programmable memory controller, coupled to said bus and to said memory, capable of providing the first set of access control signals and the second set of access control signals to said memory;

a nonvolatile memory device coupled to said bus;

a microprocessor, coupled to said bus and said memory controller, responsive to information from said nonvolatile memory device to program said memory controller to provide the first set of access control signals to said memory at a first time and the second set of access control signals to said memory at a second time.

5. A microprocessor system comprising:

a bus for transferring information;

a power supply;

a memory, coupled to said bus, comprised of a type of memory device which is selected from memory devices operable in first and second modes, said memory having a first set of access control signals for memory

devices operable in said first mode and a second set of access control signals for memory devices operable in said second mode;

a programmable memory controller, coupled to said bus and to said memory, capable of providing the first set of access control signals and the second set of access control signals to said memory;

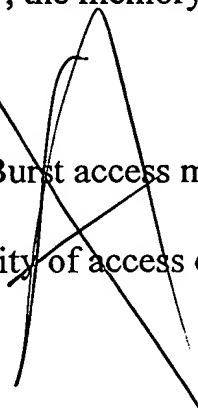
a nonvolatile memory device coupled to said bus;

a microprocessor, coupled to said bus and said memory controller, responsive to information from said memory and said nonvolatile memory device to program said memory controller to provide a set of access control signals to said memory in accordance with the type of memory device said memory is comprised of; and

a power up detection circuit coupled to said microprocessor and to said power supply, said power up detection circuit responsive to a signal from said power supply to cause said microprocessor to access said nonvolatile memory device to receive information enabling said

microprocessor to detect the type of memory device and to program the memory controller in accordance with the type of memory device said memory is comprised of.

6. A system comprising a programmable memory controller, the system adapted to receive a memory, the memory comprising:



a first bank of Burst access memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of one of either Extended Data Out memory or Fast Page Mode memory, coupled to the memory controller to receive the plurality of access control signals, wherein the memory controller drives the access control signals in a first mode to provide access to said first bank, and the memory controller drives the access control signals in a second mode to provide access to said second bank.

7. The system according to claim 6, wherein:

said second bank is interchangeably one of either Extended Data Out memory or Fast Page Mode memory.

8. A system adapted to receive a memory, the system comprising a memory controller, the memory comprising:

a first bank and a second bank, wherein the first bank and the second bank are independently interchangeably one of either a first type of memory or a second type of memory, and the memory controller controls access of the first bank in accordance with a first set of requirements for the first type and the second bank in accordance with a second set of requirements for the second type.

9. A method of determining a type of memory present in a system, comprising:

a) applying a column address to a memory;

b) writing a sequence of data patterns to the memory in a burst mode;

c) reading data from the memory in an Extended Data Out page mode beginning at the column address and advancing the column address with each Extended Data Out page mode cycle; and

d) comparing data read from the memory with data written to the memory to determine the type of memory present.

10. A method of determining a type of memory present in a system, comprising:

a) writing a sequence of data patterns to a memory in a page mode to a sequence of column addresses;

b) reading data from the memory in a burst mode; and

c) comparing data read from the memory with data written to the memory to determine the type of memory present.

11. A method of determining a type of memory present in a system, comprising:

a) writing a sequence of data patterns to a memory in a burst mode;

b) reading data from the memory in a burst mode; and

c) comparing data read from the memory with data written to the memory to determine the type of memory present.

12. In a system adapted to receive one of a plurality of different memory types, a method of determining a type of memory present, comprising:

a) writing a sequence of data patterns to a memory in a page mode to a first sequence of column addresses;

b) reading data from the memory in a page mode from a second sequence of column addresses; and

c) comparing data read from the memory with data written to the memory to determine the type of memory present.

13. The method according to claim 12 wherein:

the first sequence and the second sequence are identical.

14. The method according to claim 12 wherein:

data read from the memory is sampled at a transition time of a column address strobe.

15. The method according to claim 12wherein:

data read from the memory is sampled during a high period of a column address strobe.

16. A method of determining a type of memory present in a system, comprising:

a) writing a sequence of data patterns to a memory in a plurality of single discrete write cycles to a plurality of addresses in a first address order;

b) reading data from the plurality of addresses; and

c) comparing data read from the memory with data written to the memory to determine the type of memory present.

17. The method according to claim 16 wherein:

said step of reading data is performed in a Burst Extended Data Out mode.

18. The method according to claim 16 wherein:

said step of reading data is performed in a second address order.

19. In a system having a memory of a type which is undetermined, a method for determining the type of memory, comprising:

a) accessing the memory with control signals in a first control signal format which is incompatible with the memory; and

b) accessing the memory with the control signals in a second control signal format which is compatible with the memory.

20. A method of determining a type of a memory present in a system in response to a system initialization condition, the method comprising steps of:

a) storing a data value in the memory at an address;

b) accessing the memory in a read format at the address;

c) sampling a data output of the memory at two or more instances during said step of accessing; and

d) comparing the data output, sampled during said step of sampling, with the data value to determine the type of memory present.

21. A method of determining a type of a memory, the memory comprising a plurality of memory cells, the method comprising steps of:

a) writing a data pattern to a first cell of the memory at a first row address and a first column address in a DRAM early write access cycle format;

b) accessing the first cell and a second cell of the memory by applying at least two column address strobes in a page mode read format, a first column address strobe being applied in conjunction with the first column address, and a second column address strobe being applied in conjunction with a second column address;

c) sampling a data output from the memory subsequent to the second column address strobe being applied; and

d) comparing the data output from the memory with the data pattern to determine the type of memory.

22. The method of claim 21, further comprising a step of:

selecting a set of comparison cells from the plurality of memory cells, said set comprising the first cell and the second cell, wherein said step of selecting a set is performed prior to said step of writing a data pattern.

23. The method of claim 22, further comprising steps of:

a) programming a memory controller to access the memory in an access mode determined by the type of memory present;

b) writing, according to the access mode, a functional verification data pattern to all cells of the plurality of memory cells;

c) reading data, according to the access mode, from all cells; and

d) comparing data read to the functional verification data pattern to verify functionality of each memory cell of the memory.

24. A method of determining a type of memory, comprising:

a) writing a first data pattern and a second data pattern to a first and a second address of a memory in a page mode early write cycle format;

b) reading from the memory in a Burst Extended Data Out format comprising at least three high to low transitions of a column address strobe signal;

c) driving the column address strobe signal to a high level subsequent to said step of reading;

d) sampling a memory data output pattern subsequent to said step of driving; and

e) determining the type of memory dependent on the memory data output pattern.

25. A method to increase performance of a computer system, comprising:

a) replacing a first memory comprised of Extended Data Out type memory devices, with a second memory comprised of Burst Extended Data Out type memory devices; and

b) reinitializing the computer system to enable the computer system to determine a type of memory present, and to program a memory controller to control access of the second memory at a higher data access rate than the first memory.

add A3

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